UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,925	06/07/2004	Moriss Kung	11238-US-PA	3924

31561 7590 07/14/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,925	KUNG ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6,7,10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,7,10 and 12-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 7, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormick (US 6369448) in view of Cloud et al. (US 6525413), hereinafter Cloud.

Regarding claim 1, Fig. 4 of McCormick shows a multi-chip package module, comprising:

a second chip [412] having an active surface;

a first chip [410] positioned under the active surface of the second chip as a flip - chip structure, wherein a height of the second chip in a direction perpendicular to the active surface is defined as h1;

a plurality of first bumps [416] positioned between the active surface of the first chip and the second chip, wherein a height of the first bumps in the direction perpendicular to the active surface is defined as h2;

a plurality of contacts [414], protruding from the active surface of the first chip, wherein a height of the contacts in the direction perpendicular to the active surface is defined as h3, and values of h1, h2, and h3 are related by an in-equality of $h3 \geq hi + h2$; and

an underfill film [418] made from am insulating material formed over the active surface of the first chip and the second bump.

Fig. 4 of McCormick shows most aspects of the instant invention except the stacked second bumps and the contacts. Fig. 12 of Cloud shows stacked second bumps [117] and the contacts [114b].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Cloud into the device of McCormick in order to have the second bump stacked and the contacts for secure connection.

Regarding claim 4, Fig. 4 of McCormick shows that an insulating material [418] over the active surface of the first chip that encloses the first bumps and the contacts.

Regarding claim 7, Fig. 4 of McCormick shows a multi-chip package structure, comprising:

a substrate [402];

a plurality of contacts [414];

a first chip [410] having an active surface that faces the substrate, wherein the contacts are positioned between the first chip and the substrate, and a distance between the substrate and the active surface in a direction perpendicular to the active surface is defined as d;

a second chip [412] positioned between the first chip and the substrate, wherein a height of the second chip in the direction perpendicular to the active surface is defined as h1; and

a plurality of first bumps [422] positioned between the active surface of the first chip and the second chip for electric connection, wherein a height of the first bumps in the

direction perpendicular to the active surface is defined as h2 and values of h1, h2 and d are related by an inequality of $d \geq hi + h2$.

Fig. 4 of McCormick shows most aspects of the instant invention except the stacked second bumps and the contacts. Fig. 12 of Cloud shows stacked second bumps [117] and the contacts [114b].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Cloud into the device of McCormick in order to have the second bump stacked and the contacts for secure connection.

Regarding claim 10, Fig. 4 of McCormick shows that an insulating material [418] over the active surface of the first chip that encloses the first bumps and the contacts.

Regarding claim 12, Fig. 4 of McCormick shows that a height of the contacts in the direction perpendicular to the active surface is defined as h3 and values of hi, h2 and h3 are related by an inequality of $h3 \geq h1 + h2$.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein et al. (US Pat. Pub. 2004/0145051), hereinafter Klein in view of Cloud Regarding claim 1, Fig. 9A of Klein shows a multi-chip package module, comprising:

Regarding claim 7, Fig. 9A of Klein shows a multi-chip package structure, comprising:

a substrate (paragraph [0092]);

a plurality of contacts [11, 118];

a first chip [12] having an active surface that faces the substrate, wherein the contacts are positioned between the first chip and the substrate, and a distance between the substrate and the active surface in a direction perpendicular to the active surface is defined as d;

a second chip [14-1] positioned between the first chip and the substrate, wherein a height of the second chip in the direction perpendicular to the active surface is defined as h1; and

a plurality of first bumps [44] positioned between the active surface of the first chip and the second chip for electric connection, wherein a height of the first bumps in the direction perpendicular to the active surface is defined as h2 and values of h1, h2 and d are related by an inequality of $d \geq hi + h2$.

Fig. 9A of Klein shows most aspects of the instant invention except the stacked second bumps and the contacts. Fig. 12 of Cloud shows stacked second bumps [117] and the contacts [114b].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Cloud into the device of McCormick in order to have the second bump stacked and the contacts for secure connection.

Regarding claim 8, Fig. 9A of Klein shows that each of the contacts comprises a plurality of stacked second bumps [22, 118].

Claims 6 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormick in view of Cloud as applied to claims 6 and 7 above, and further in view of Venkateshwaran et al. (US 6339253), hereinafter Venkateshwaran.

Regarding claim 6, the combined teachings of McCormick and Cloud show most aspects of the instant invention except "a third chip and a plurality of third bumps, wherein the third chip is positioned over the active surface of the first chip as a flip chip structure, the third bumps are positioned between the active surface of the first chip and the third chip, a height of the third chip in the direction perpendicular to the active surface being defined as h4, a height of the third bumps in the direction perpendicular to the active surface being defined as h5, and values of h3, h4 and h5 are related by an in-equality of $h3 \geq h4 + h5$." Fig. 7 of Venkateshwaran shows a multi-chip package structure, comprising a third chip [704] and a plurality of third bumps, wherein the third chip is positioned over the active surface of the first chip, the third bumps are positioned between the active surface of the first chip and the third chip, a height of the third chip in the direction perpendicular to the active surface being defined as h4, a height of the third bumps in the direction perpendicular to the active surface being defined as h5, and values of h3, h4 and h5 are related by an in-equality of $h3 \geq h4 + h5$.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Venkateshwaran into the device of McCormick and Cloud in order to have "a third chip and a plurality of third bumps, wherein the third chip is positioned over the active surface of the first chip as a flip chip structure, the third bumps are positioned between the active surface of the first chip and the third chip, a height of the third chip in the direction perpendicular to the active surface being defined as h4, a height of the third bumps in the direction perpendicular to the active surface being defined as h5, and

values of h3, h4 and h5 are related by an in-equality of h3 $\geq$ h4 + h5" for a compact package structure.

Regarding claim 13, the combined teachings of McCormick and Cloud show most aspects of the instant invention except "a third chip and a plurality of third bumps such that the third chip is positioned between the first chip and the substrate, as well as the third bumps are positioned between the first chip and the third chip to connect together as a flip chip structure, wherein a height of the third chip in the direction perpendicular to the active surface is defined as h4 and a height of the third bumps in the direction perpendicular to the active surface is defined as h5, and values of d, h4 and h5 are related by an inequality of d $\geq$ h4 + h5." Fig. 7 of Venkateshwaran shows a multi-chip package structure, comprising a third chip [704] and a plurality of third bumps such that the third chip is positioned between the first chip [701] and the substrate [700], as well as the third bumps are positioned between the first chip and the third chip to connect together, wherein a height of the third chip in the direction perpendicular to the active surface is defined as h4 and a height of the third bumps in the direction perpendicular to the active surface is defined as h5, and values of d, h4 and h5 are related by an inequality of d $\geq$ h4 + h5

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Venkateshwaran into the device of McCormick/Cloud in order to have "a third chip and a plurality of third bumps such that the third chip is positioned between the first chip and the substrate, as well as the third bumps are positioned between the first chip and the third chip to connect together as a flip chip structure, wherein a height of the third chip in the direction perpendicular to the active

surface is defined as h4 and a height of the third bumps in the direction perpendicular to the active surface is defined as h5, and values of d, h4 and h5 are related by an inequality of $d \geq h4 + h5$" for a compact package structure.

Regarding claim 14, Fig. 4 of McCormick shows that a height of the contacts in the direction perpendicular to the active surface is defined as h3 and values of h3, h4 and h5 are related by an inequality of $h3 \geq h4 + h5$.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

Steven Loke
Primary Examiner
Steven Loke